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What Is Claimed Is:

1. A method of forming dielectric layers with various thicknesses on a substrate, comprising the steps of:

providing a first device region and a second device region on the substrate;

growing a first oxide layer on the substrate ;

depositing a dielectric layer with a first thickness on the first oxide layer;

removing the dielectric layer and the underlying first oxide layer on the second device region to expose the substrate; and

growing a second oxide layer with a second thickness less than the first thickness on the substrate of the second device region.

2. The method of claim 1, wherein the substrate further comprises a third device region.

3. The method of claim 2, wherein the third device region is a core device region for low voltage operation.

4. The method of claim 2, further comprising the steps of:

removing the dielectric layer and the underlying first oxide layer on the third device region to expose the substrate; and

growing a third oxide layer with a third thickness less than the first thickness on the substrate of the third device region and on the second oxide layer.

5. The method of claim 4, wherein third oxide layer is grown by thermal oxidation.

6. The method of claim 4, wherein the third thickness is about 30 to 60Å.

7. The method of claim 1, wherein the first device region is a power device region for high voltage operation.

8. The method of claim 1, wherein the second device region is an I/O device region for low voltage operation.

9. The method of claim 1, wherein the first oxide layer is grown by thermal oxidation.

10. The method of claim 1, wherein the dielectric layer is a high temperature oxide layer formed by CVD.

11. The method of claim 1, wherein the first thickness is about 300 to 3000Å.

12. The method of claim 1, wherein second oxide layer is grown by thermal oxidation.

13. The method of claim 1, wherein the second thickness is about 40 to 70Å.

14. A method of forming gate dielectric layers with various thicknesses on a substrate, comprising the steps of:

providing a first active region and a second active region on the substrate;

forming a first thermal oxide layer on the substrate;

depositing a blanket dielectric layer with a first thickness overlying the substrate;

forming a first masking layer overlying the substrate except over the second active region;

etching the dielectric layer and the underlying first thermal oxide layer on the second active region using the first masking layer as an etch mask to expose the substrate;

removing the first masking layer;

forming a second thermal oxide layer with a second thickness less than the first thickness on the second active region; and

forming a first gate on the dielectric layer on the first active region and a second gate on the second thermal oxide layer on the second active region.

15. The method of claim 14, wherein the substrate further comprises a third active region.

16. The method of claim 15, wherein the third active region is separated from the second active region by a shallow trench isolation region.

17. The method of claim 15, wherein before forming the first and second gates, further comprising the steps of:

forming a second masking layer overlying the substrate except over the third active region;

removing the dielectric layer and the underlying first thermal oxide layer on the third active region to expose the substrate;

removing the second masking layer; and

forming a third thermal oxide layer with a third thickness less than the first thickness on the third active region and on the second thermal oxide layer.

18. The method of claim 17, wherein the second masking layer is a photoresist layer.

19. The method of claim 17, wherein the step of forming the first and second gates further comprises forming a third gate on the third thermal oxide layer on the third active region.

20. The method of claim 17, wherein the third thickness is about 30 to 60Å.

21. The method of claim 14, wherein the first active region and the second active region are separated by a shallow trench isolation region.

22. The method of claim 14, wherein the dielectric layer is a high temperature oxide layer formed by CVD.

23. The method of claim 14, wherein the first thickness is about 300 to 3000Å.

24. The method of claim 14, wherein the first masking layer is a photoresist layer.

25. The method of claim 14, wherein the second thickness is about 40 to 70Å.

26. A method of forming an integrated circuit having gate oxide layers with multiple thicknesses, comprising the steps of:

providing a substrate having a first active region, a second active region, and a third active region;

performing a first oxidation to form a first oxide layer on the substrate;

depositing a blanket high temperature oxide layer with a first thickness overlying the substrate;

forming a first photoresist layer on the high temperature oxide layer except over the second active region;

etching the high temperature oxide layer and the underlying first oxide layer on the second active region using the first photoresist layer as an etch mask to expose the substrate;

removing the first photoresist layer;

performing a second oxidation to form a second oxide layer with a second thickness less than the first thickness on the second active region;

forming a second photoresist layer overlying the substrate except over the third active region;

removing the high temperature oxide layer and the underlying first oxide layer on the third active region to expose the substrate;

removing the second photoresist layer;

performing a third oxidation to form a third oxide layer with a third thickness less than the first thickness

on the third active region and on the second oxide layer on the second active region; and

forming a first gate on the high temperature oxide layer on the first active region, a second gate on the second oxide layer on the second active region, and a third gate on the third thermal oxide layer on the third active region.

27. The method of claim 26, wherein the first, second, and third active regions are separated by a shallow trench isolation region.

28. The method of claim 26, wherein the first thickness is about 300 to 3000Å.

29. The method of claim 26, wherein the second thickness is about 40 to 70Å.

30. The method of claim 26, wherein the third thickness is about 30 to 60Å.

31. The method of claim 26, wherein the high temperature oxide layer is formed by CVD.